REMARKS

Applicant has reviewed and considered the Office Action mailed on April 22, 2003, and the references cited therewith.

Claims 10, 16, 17, 22, 23, 29, 31, 32, 33, 37, 40, 44, and 45 are amended, no claims are canceled, and no claims are added; as a result, claims 10, 11, 13-18, 20-24, 26-38, and 40-45 are now pending in this application. The amendments to the claims are fully supported by the specification as originally filed. No new matter has been introduced. Applicant respectfully requests reconsideration of the above-identified application in view of the amendments above and the remarks that follow.

Applicant's representative thanks Examiner Tra for taking the time to speak with him on 16 June 2003. Examiner Tra was contacted regarding the lack of references regarding the rejections to claim 16. No agreement regarding claim 16 was reached.

Applicant respectively requests that the finality of the Office Action be withdrawn since the rejections to claim 16 were not supported by a reference or an affidavit as required by 37 C.F.R. § 1.104(d)(2), as previously requested in Applicant's response mailed 20 February 2003.

Claims 16, 22, and 31 are amended to be written in independent form and not with regard to a prior art rejection.

Claims 10, 17, 23, 29, 32, 33, 37, 44 and 45 find support, for example, in the specification on page 12, lines 14-26.

First §103 Rejection of the Claims

Claims 10, 11, 13, 14, 16-18, 20-24, 26, 27, 29-38 & 44-45 were rejected under 35 USC § 103(a) as being unpatentable over Austin (U.S. No. 5,982,690) in view of Chung (U.S. No. 5,442,209). Applicant traverses these grounds for rejection.

Applicant does not admit that the Austin patent is prior art to the present invention and reserves the right to swear behind this patent at a later date. Nevertheless, Applicant also submits that the Austin patent is distinguishable from the present invention.

Claim 16 is amended to be written in independent form.

Applicant can not find in Austin or in Chung a teaching or suggestion of a latch circuit that is able to output a full output sense voltage in less than 10 nanoseconds (ns), as recited in

claim 16. Austin appears to deal with a static, low-power differential sense amplifier having cross-linked transistors to reduce current power consumption. *See, for instance, column 2, lines 42-46.* Further, Austin appears to rely on the architecture of his disclosed circuit to reduce current power consumption, and not on the structure of individual transistors, other than to note that a series of transistors are all sized substantially identically for power dissipation purposes. *See, for instance, column 7, lines 65- column 8, line 2.* Sizing transistors identically does not teach of suggest configuring transistors in a latch circuit such that the latch circuit is able to output a full output sense voltage in less than 10 nanoseconds (ns), as recited in claim 16.

Chung in a nonanalogous art related to synapse transistors deals with a multiple gate MOS transistor to be used to implement a neural network. A result of Chung's synapse transistor includes having multiple transistors with a common drain and a common source, which reduces the overall amount of a chip used to fabricate the multiple synapse transistors, though Chung does not appear to teach or suggest reducing the size of an individual transistor. Applicant can not find in Chung a teaching or suggestion for configuring such transistors for a latch circuit to output a full output sense voltage in less than 10 nanoseconds. Thus, Chung does not cure the abovementioned deficiencies of Austin.

The Office Action states that

> it is well known in the art that the speed for the amplifier circuit dependent on the size of the transistors in the amplifier. Furthermore, Austin amplifier circuit having similar structure as Applicant amplifier circuit figure 2A. Therefore, Austin circuit is able to provide a full output of the sense voltage less than 10 nanoseconds depend on the size of the transistors in the amplifier. It is would have been obvious to one having ordinary skill in the art to modify the size of Austin amplifier circuit in order for the circuit to providing an output less than 10 nanoseconds because it is seen as a design choice.

Applicant respectfully disagrees for several reasons. Though reducing the size of a given transistor may or may not reduce the speed of that transistor, such a disclosure doe not teach or suggest that a latch circuit is able to output a full output sense voltage in less than 10 nanoseconds. Other factors may contribute to the speed of transistor in a latch circuit as used in claim 16. Further, the Office Action has provided no references to support the Office Action position that arbitrarily reducing transistor size teaches or suggests a latch circuit able to output a

full output sense voltage in less than 10 nanoseconds, as recited in claim 16. In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *Schenck v. Nortron Corp.*, 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983); *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985); MPEP § 2141.02.

Additionally, having a similar architecture does not teach or disclose that Austin's circuit operates in the same manner as the latch of claim 16. Though Austin may arguably have a similar circuit architecture, since Austin does not appear to have transistor structures as in claim 16, Austin does not teach or suggest the latch configured as recited in claim 16. The architecture of Austin's circuit is used to reduce current power consumption by having a transistor that is on coupled to another transistor that is off to provide an output such that there is minimal current flow during switching with transistors sized relatively identically. Austin appears to lack a teaching or suggestion regarding the structure of the transistors that have a configuration related to speed of operation of the latch circuit. On the other hand, Applicant has provided an embodiment supporting claim 16 in the specification, for example, on page 12, lines 14-19. Applicant submits that one of ordinary skill in the art would have to apply the teaching of Applicant's specification to modify Austin's circuit to teach or suggest the latch of claim 16, which is impermissible hindsight.

Further, Applicant submits that a latch circuit able to output a full output sense voltage in less than 10 nanoseconds (ns), as recited in the whole of claim 16 is not an obvious design choice. No reference or support has been provided to show that a latch circuit "able to output a full output sense voltage in less than 10 nanoseconds (ns)," as recited by claim 16, is a member of a known group of devices or device characteristic from which a design choice can be made. A device having an element or characteristic that can be quantitatively recited does not make that element or its application as part of a claimed device a design choice subject to obviousness.

With respect to claim 42, the Office Action further stated "it is also seen as a design choice for designing the output speed of the sense amplifier to be able to output a full output

sense voltage in less than 10 nanoseconds (ns) dependent upon particular environment of use to ensure optimum performance." This is a conclusionary statement without support that a sense amplifier able to output a full output sense voltage in less than 10 nanoseconds (ns) is an obvious design choice to ensure optimum performance. A particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation. *In re Antonie*, 559 F.2d 618, 195 USPQ 6 (CCPA 1977) See also *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980) See, MPEP 2144.05. The Office Action has provided no reference to support the position that the structures able to output a full output sense voltage in less than 10 nanoseconds (ns) as recited in the instant claims have characteristics that are result-effective. Thus, applicant submits that the structures able to output a full output sense voltage in less than 10 nanoseconds (ns) as recited in the instant claims are not obvious design choices.

Since Austin, Chung, and other cited references do not teach or suggest all the elements as recited in claim 16, Applicant submits that claim 16 is patentable under §103 over Austin and Chung.

In addition, Applicant respectfully submits that the Office Action did not make out a proper *prima facie* case of obviousness since Austin and Chung are nonanalogous art and there combination is not proper.

"In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992). See also *In re Deminski*, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986); *In re Clay*, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992) ("A reference is reasonably pertinent if, even though it may be in a different field from that of the inventor's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem."); and *Wang Laboratories Inc. v. Toshiba Corp.*, 993 F.2d 858, 26 USPQ2d 1767 (Fed. Cir. 1993). See, M.P.E.P. 2141.01.

Austin deals with sense amplifiers relating to static, low-power differential sense amplifiers as used in conventional memory cells such as in random access memories (RAMs). *See Austin, column one.* In contrast, Chung deals with a synapse MOS transistor that is useful in neural networks. *See Chung, column one.*

Further, Austin deals with the problem of power consumption in memory cells as noted in column one of Austin and reaffirmed in Austin's disclosure, for example, in column 8, lines 64-67: "[c]onsequently, power consumption according to the present invention is greatly reduced for applications in which output read data sees a large capacitance."

In contrast, Chung deals with the problem of "the reduction of the number of connections between neurons, the multiplication of weights, and the summing of the weights at each node," *See, Chung column 1, lines 57-61.* A result of Chung's solution to his stated problem is a synapse MOS transistor that results in a reduced chip area, See, *Chung column 3, lines 34-36.* However, this size reduction is not the problem addressed by Chung.

Applicant submits that Chung's a synapse transistor for implementing a neural network does not logically commended itself to an inventor's attention in considering Austin's problem of power consumption. In considering pertinence of nonanalogous art it appears from *In re Wang*, as noted in the MPEP, that one looks at the problems to be solved in the references and not at a result in providing a solution to one of the references. Therefore, Applicant believes that the Austin and Chung references are nonanalogous art and that their combination is not proper to any of the instant claims.

Claims 22 and 31 are amended to be written in independent form. Claims 22 and 31 recite similar elements as claim 16 and are patentable over Austin and Chung for the reasons stated above in addition to the elements of these claims.

With respect to independent claims 10, 17, 23, 29, 32, 33, 37, 44 and 45, as amended, Applicant can not find in Austin or in Chung a teaching or suggestion of a dual-gated MOSFET or transistor having a threshold voltage ranging from about 0.3 V to about 0.35V, as recited in these claims. Therefore, Austin and a combination of Austin with Chung do not teach or suggest all the elements of these independent claims. Thus, Applicant submits that claims 10, 17, 23, 29, 44, and 45 are patentable over Austin in view of Chung.

Claims 11, 13, and 14, claims 18, and 20-21, claims 24, 26-28, claim 30, claims 34-36, and claim 38 are dependent on claims 10, 17, 23, 29, 33, and 37, respectively, and are patentable over Austin in view of Chung for the reasons stated above in addition to the elements of the claims.

Applicant respectively requests withdrawal of these rejections to claims 10, 11, 13, 14, 16-18, 20-24, 26, 27, 29-38 & 44-45, and reconsideration and allowance of these claims.

Second §103 Rejection of the Claims

Claim 15 was rejected under 35 USC § 103(a) as being unpatentable over Austin (U.S. No. 5,982,690) in view of Chung (U.S. No. 5,442,209) and Ang et al. (U.S. No. 5,942,918). Applicant traverses these grounds for rejection.

Applicant does not admit that the Austin patent is prior art to the present invention and reserves the right to swear behind this patent at a later date. Nevertheless, Applicant also submits that the Austin patent is distinguishable from the present invention.

Claim 15 is dependent on claim 10, where claim 10 recites "the dual-gated MOSFET having a threshold voltage ranging from about 0.3 V to about 0.35V." Applicant can not find in Austin or in Chung a teaching or suggestion of a dual-gated metal-oxide semiconducting field effect transistor as recited in claims 10 and 15. Ang et al. (hereafter Ang) does not cure the abovementioned deficiencies in Austin, Chung, or, as previously discussed, the improper combination of Austin with Chung.

Applicant submits that for the reasons stated above claim 15 is patentable over Austin in view of Chung and in view of Ang. Applicant requests withdrawal of this rejection to claim 15, reconsideration and allowance of claim 15.

Third §103 Rejection of the Claims

Claims 28 & 40-43 were rejected under 35 USC § 103(a) as being unpatentable over Kaneko et al. (U.S. No. 6,069,828) in view of Austin (U.S. No. 5,982,690) and Chung (U.S. No. 5,442,209). Applicant traverses these grounds for rejection.

Applicant does not admit that the Austin patent is prior art to the present invention and reserves the right to swear behind this patent at a later date. Nevertheless, Applicant also submits that the Austin patent is distinguishable from the present invention.

Claim 28 is dependent on claim 23, where claim 23, as amended, recites a "dual-gated NMOS having a threshold voltage ranging from about 0.3 V to about 0.35V." Applicant can not find in Austin or a teaching or suggestion of a dual-gated NMOS transistor as recited in claims 23 and 28. Chung deals with reducing the number of connections between neurons in a neutral network by using transistors that have a common drain and common source. Applicant can not find or in Chung a teaching or suggestion of a dual-gated MOSFET having a threshold voltage ranging from about 0.3 V to about 0.35V as recited in claims 23 and 28. Therefore, Chung does not cure the abovementioned deficiencies of Austin. Additionally, as previously discussed, combining Austin with Chung is improper.

The Office Action applies Kaneko et al. (hereafter Kaneko) noting that Kaneko "shows all elements of the claim except for the detail of the sense amplifier." Therefore, Kaneko also does not cure the deficiencies of Austin. Thus, Austin in view of Chung and Kaneko does not teach or suggest all the elements of claim 28.

Claim 40 recites "dual-gated transistor having a threshold voltage ranging from about 0.3 V to about 0.35V." As stated above, Kaneko does not cure the abovementioned deficiencies of Austin and Chung. Thus, Austin in view of Chung and Kaneko does not teach or suggest all the elements of claim 40.

Claims 41-43 are dependent on claim 40 and are patentable over Kaneko in view of Austin and Chung for the reasons stated above plus the elements of these claims.

Applicant respectively requests withdrawal of these rejections of claims 28 and 40-43, and reconsideration and allowance of these claims.

Assertion of Pertinence

Applicant need not respond to the assertion of pertinence stated for the references cited but not relied upon by the Office Action since these references are not made part of the rejections in this Office Action. Applicant is expressly not admitting to this assertion and reserves the right to address the assertion should it form part of future rejections

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney 612-371-2157 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
612-371-2157

Date 23 June 2003 By David R. Cochran

David R. Cochran
Reg. No. 46,632

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 23 day of June, 2003

Gina M. Uphus Gina Uphus

Name Signature